

Notice of Allowability

Application No.

10/720,261

Examiner

Henry Baron

Applicant(s)

SUND ET AL.

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 11/25/2003.
2. ☒ The allowed claim(s) is/are 1-5.
3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892) ✓
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date: _____ ✓
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date: _____
7. ☒ Examiner's Amendment/Comment ✓
8. ☒ Examiner's Statement of Reasons for Allowance ✓
9. ☐ Other _____

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EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with David J. Cushing on July 16th, 2007.

The application has been amended as follows:

Abstract

A method for handling data between a clock and data recovery system CDR and a data processing unit DP of a telecommunications network node TNN of an asynchronous communications network, using a bit rate adaptation circuit BAS, the bit rate adaptation system BAS ~~comprising~~including a memory unit MEM with a write process circuit Wp controlled by the recovered clock Rclk and a read process circuit Rp controlled by the local clock Lclk where ~~in~~ the bit rate adaptation system BAS also ~~comprises~~includes a pointer synchronization controller PSC which, depending on the data detected on the input data signal Dib1 of the bit rate adaptation system BAS, sets the read and write pointers to a fixed initial address value. A Clock and Data Recovery system and a telecommunications network node TNN of an asynchronous network, which ~~comprise~~include a bit adaptation circuit BAS according to the invention, are also disclosed.

Listing of Claims:

1. (currently amended) A method for handling data between a Clock and Data Recovery (CDR) circuit and a data processing unit of a telecommunications network node of an asynchronous network, using a bit rate adaptation system comprising a memory unit ~~with a memory stack and a write process circuit and a read process circuit~~, and Pointer Synchronization Controller, said memory unit having a

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memory stack and a write process circuit and a read process circuit, said method comprising the steps of:

the CDR passing recovered data and recovered clock signals to the bit rate adaptation system and the bit rate adaptation system handling the data to the processing unit at a rate indicated by a local node clock;

the write process circuit, controlled by the recovered clock, incrementing a write pointer and writing the recovered data into the memory address indicated by said write pointer, and the read process circuit controlled by the local clock incrementing a read pointer and reading the recovered data from the memory address indicated by said read pointer, both pointers running free until the end of a data frame; and

the pointer synchronization controller monitoring the recovered data signal to detect guard bands between data frames and bit synchronization fields and, depending on this information, acting on the pointers of the memory unit

wherein

upon detecting the guard band between data frames, the write pointer is set to a predetermined fixed initial address; and

upon detecting the bit synchronization field of the input data frame, the read pointer is set to said write pointer fixed initial address.

2. (currently amended) A bit rate adaptation circuit for handling data between a Clock and Data Recovery circuit and a processing unit of a telecommunications network node of an asynchronous network, comprising

a memory unit with a memory stack, a read process circuit Rp and a write process circuit Wp, built in such a manner so that the write process circuit, controlled by a recovered clock input coming

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from the Clock and Data Recovery circuit, increments a write pointer and writes data into the memory address indicated by said write pointer, and the read process circuit, controlled by a local node clock, increments a read pointer and reads data from the memory address indicated by said read pointer; and

a pointer synchronization controller built in such a manner so that it is able to monitor the recovered data signal and detect guard bands between data frames and bit synchronization fields and, depending on this information, is able to act on the pointers of the memory unit MEM,

wherein the pointer synchronization controller is further built such that it sets the write pointer to a predetermined fixed initial address value when a guard band is detected, and sets the read pointer to said fixed initial address value of the write pointer when a bit synchronization field is detected.

3. (currently amended) A Clock and Data Recovery system of a telecommunications network node of an asynchronous network comprising a Clock and Data Recovery circuit and thea bit rate adaptation circuit according to claim 2.

4. (currently amended) A telecommunications network node of an asynchronous network comprising a bit rate adaptation circuit according to claim 2. for handling data between a Clock and Data Recovery circuit and a processing unit of a telecommunications network node of an asynchronous network, comprising

a memory unit with a memory stack, a read

process circuit Rp and a write process circuit Wp, built in such a manner so that the write process circuit, controlled by a recovered clock input coming from the Clock and Data Recovery circuit, increments a write pointer and writes data into the memory address indicated by said write pointer, and the read process circuit, controlled by a local node clock, increments a read pointer and reads data from the memory address indicated by said read pointer; and

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a pointer synchronization controller built in such a manner so that it is able to monitor the recovered data signal and detect guard bands between data frames and bit synchronization fields and depending on this information is able to act on the pointers of the memory unit MEM,

wherein the pointer synchronization controller is further built such that it sets the write pointer to a predetermined fixed initial address value when a guard band is detected, and sets the read pointer to said fixed initial address value of the write pointer when a bit synchronization field is detected or a Clock and Data Recovery system according to claim 3.

5. (new) A telecommunications network node of an asynchronous network comprising a Clock and Data Recovery System according to claim 3.

Reason for Allowance

Claims 1-5 are allowed.

The following is an examiner's statement of reasons for allowance:

Boles (U.S. Patent Application 2004/0057539) teaches a CDR where the recovered data and clock are used to write to a FIFO and a local clock is used to read the data before post-processing. Boles FIFO uses the local and recovered clocks to independently increment read and write pointers and derives an offset by subtracting the read and write pointers. (Figure 4 and 3:[0029] and 3:[0030]). Wen (U.S. Patent 6,212,122) teaches of a dual port RAM (DPRAM) where a synchronization circuit is used to coordinate address pointers i.e. read and write pointers across clock domains. (2: [0014-0025]). However neither Boles, Wen, or any other prior art teaches of a pointer synchronization circuit that sets a write pointer to a specific address e.g. '0' when it detects a guard band and aligns the read pointer with the write pointer when it detects a synchronization bit sequence. It is on the basis of this teaching that the claims are allowed.

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Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry Baron whose telephone number is (571) 270-1748. The examiner can normally be reached on 7:30 AM to 5:00 PM E.S.T. Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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